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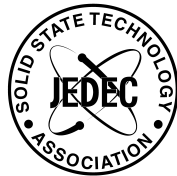
I/O Drivers and Receivers with Configurable Communication Voltage, Impedance, and Receiver Threshold

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I/O DRIVERS AND RECEIVERS WITH CONFIGURABLE COMMUNICATION VOLTAGE, IMPEDANCE, AND RECEIVER THRESHOLD

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Foreword

This standard attempts to aid the design of electronic Systems comprised of components that operate at several different supply voltages. This standard is developed around the following principles:

If two or more chips of different voltages are in communication, the communication voltage should be equal to the lowest supply voltage. Thus drivers and receivers should be configurable in their communication voltage.

The reference or switch point of the receiver should track with the communication voltage. The reference may be either externally or internally supplied. Thus receiver mode should be configurable.

The impedance of the driving circuits should be matched to the load, independent of the communication voltage. Thus the driving circuit impedance should be configurable.

Introduction

This standard is the compilation of 4 separate JEDEC documents covering respectively configurable I/O voltage, receiver type and switchpoint, and driver impedance.

The intent of sections 1 and 2 is to guide designs of interface driver and receiver circuits to allow communication between chips of different supply voltages VDD. Although the communication voltage VDDQ may exceed the supply voltage, this standard is intended to guide designs of interface circuits that operate with VDDQ at or less than VDD. The use of circuits which operate at more than one well defined interface voltage will allow communication between chips of different supply voltages with a minimum effect on I/O delay, speed, reliability, or chip area. These sections cover power supply voltages VDD from 3.3 V to 1.8 V and 1.5 V to 0.8 V.

The intent of section 3 is to guide designs of interface receiver circuits to allow operation with more than one method of defining the receiver switch point or reference voltage. As circuit speeds increase and circuit operating voltages decrease, different circuit techniques may be employed. Broadly described, the techniques can be separated into two types: those circuits that use an external voltage reference to define a switch point, and those circuits that use an internal reference, contained wholly within the chip, to define a receiver switch point. This section covers both types of receivers and describes how to switch from one type to the other. It is expected that the switch from externally referenced receivers to internally referenced receivers will in general result in some loss of common mode noise rejection.

Introduction (cont'd)

The intent of section 4 is to improve the specification of semiconductor off-chip driver circuits. The improved specification will allow a better match of circuit driver performance and output load. In addition the section allows for selectable driver strength, thus allowing a semiconductor device to operate optimally under different output loading conditions. In particular, this specification will refer to the value of a driver circuit output impedance, and is intended for matching to the impedance of transmission line structures for high speed communication between semiconductor devices.

I/O DRIVERS AND RECEIVERS WITH CONFIGURABLE COMMUNICATION VOLTAGE, IMPEDANCE, AND RECEIVER THRESHOLD

(From Council Ballots JCB-97-59, JCB-97-60, JCB-97-61, and JCB-97-62, formulated under the cognizance of the JC-16 Committee on Electrical Interface and Power Supply Standards for Electronic Components.)

1 Flexible I/O interface supply voltage: I

1.1 Nominal supply voltages and I/O parametrics

The supply voltage of semiconductors is expected to decrease to below one volt over the next several years. As a result, it is expected that systems will be developed utilizing semiconductor chips of different supply voltages. Table 1-1 below shows how we expect the supply voltage, and hence the maximum communication voltage, to migrate.

Table 1-1 — Expected migration of supply voltages and receiver reference voltage

VDD,VDDQ (Volts)	3.3	2.5	1.8	1.5
Vref (Volts)	1.5	1.25	0.9	0.75

The relationship is approximately $V_{ref} = VDDQ/2$.

To facilitate communication between chips of different supply voltages, we have specified the interface parametrics. They are separated into a High Performance Class (Class A) and a Wide Margin Class (Class B). The high performance interface specifications are primarily intended for high speed communication where sensitive receivers, perhaps based on externally referenced differential amplifiers, and are used to reduce the cycle time at the expense of power. The wide margin interface specifications are intended primarily for slower speed communication where power is reduced and where less sensitive, more noise tolerant receivers can be used, perhaps based on internally referenced circuits. The voltage of an entry, V_{ih} or V_{il} , in table 2 is (calculated by using the nominal values of VDD and VDDQ of the receiver. The voltage, V_{ih} or V_{il} , when expressed in volts, is valid to 2 decimal places ($\pm 10\text{mV}$). The V_{ih} and V_{il} of table 1-2 are expected to hold for all operating conditions.

1.1 Nominal supply voltages and I/O parametrics (cont'd)

Table 1-2 — Nominal Interface Parametrics

Class A (High Performance)				Class B (Wide Margin)			
Vih(DC)_min	=	Vref	+ 0.07 * VDD	Vih(DC)_min	=	Vref	+ 0.14 * VDD
Vih(DC)_max	=	VDDQ	+ 0.10 * VDD	Vih(DC)_max	=	VDDQ	+ 0.10 * VDD
Vil(DC)_max	=	Vref	- 0.07 * VDD	Vil(DC)_max	=	Vref	- 0.14 * VDD
Vil(DC)_min	=		VSS	Vil(DC)_min	=		VSS
Vih(AC)_min	=	Vref	+ 0.14 * VDD	Vih(AC)_min	=	Vref	+ 0.25 * VDD
Vih(AC)_max	=	VDDQ	+ 0.15 * VDD	Vih(AC)_max	=	VDDQ	+ 0.15 * VDD
Vil(AC)_max	=	Vref	- 0.14 * VDD	Vil(AC)_max	=	Vref	- 0.25 * VDD
Vil(AC)_min	=	VSS	- 0.15 * VDD	Vil(AC)_min	=	VSS	- 0.15 * VDD

Although it is commonplace to standardize Output driver current and output driver voltages (Voh, Vol), this standard will refer to output driver impedances. Through reference to driver impedance the driver characteristics will become easier to define and the resultant driver behavior under various loading conditions will be easier to predict. For the expected values for driver impedance and the parametrics associated with the drivers (see section 4).

1.2 Interoperability

It is expected that a group of devices of different supply voltages VDD will communicate with a common communication voltage VDDQ which is equal to or less than VDD_low the lowest supply voltage of the group. Although it is desirable that chips of supply voltage VDD operate over the largest possible range of VDDQ, to meet this standard it is sufficient that chips of VDD specified in table 1-3 support communication at the associated values of VDDQ, with the Vil, Vih specifications of table 1-2.

Table 1-3 — Relationship between VDD, VDDQ, and Vref

VDD	VDDQ	Vref
3.3 V	3.3 V, 2.5 V	1.5 V, 1.25 V
2.5 V	2.5 V, 1.8 V	1.25 V, 0.9 V
1.8 V	1.8 V, 1.5 V, 1.2 V	0.9 V, 0.75 V, 0.6 V

The relationship is roughly $VDD \geq VDDQ \geq 0.6 \times VDD$

1.2 Interoperability (cont'd)

Similarly the I/O drivers associated with a semiconductor device operating with external voltage VDD must be capable of providing an output voltage satisfying the input requirements V_{il} and V_{ih} of table 1-2 for a receiver configured for any associated VDDQ in table 1-3, at the specified impedance. Separate VDDQ pins are recommended but not required. Separate VSS and VSSQ pins are acceptable but not required.

2 Flexible I/O interface supply voltage: II

2.1 Nominal supply voltages and I/O parametrics

The supply voltage of semiconductors is expected to decrease to below one volt over the next several years. As a result, it is expected that systems will be developed utilizing semiconductor chips of different supply voltages. Table 2-1 below shows how we expect the supply voltage, and hence the maximum communication voltage, to migrate.

Table 2-1 — Expected migration of supply voltages and receiver reference voltage

VDD,VDDQ (Volts)	1.5	1.2	1.0	0.8
Vref (Volts)	0.75	0.6	0.5	0.4

The relationship is approximately $V_{ref} = VDDQ/2$.

To facilitate communication between chips of different supply voltages, we have specified the interface parametrics. They are separated into a High Performance Class (Class A) and a Wide Margin Class (Class B). The high performance interface specifications are primarily intended for high speed communication where sensitive receivers, perhaps based on externally referenced differential amplifiers, and are used to reduce the cycle time at the expense of power. The wide margin interface specifications are intended primarily for slower speed communication where power is reduced and where less sensitive, more noise tolerant receivers can be used, perhaps based on internally referenced circuits. The voltage of an entry, V_{ih} or V_{il} , in table 2-2 is calculated by using the nominal values of VDD and VDDQ of the receiver. The voltage, V_{ih} or V_{il} , when expressed in volts, is valid to 2 decimal places (+/- 10mV). The V_{ih} and V_{il} of table 2-2 are expected to hold for all operating conditions.

2.1 Nominal supply voltages and I/O parametrics (cont'd)

2-2 — Nominal Interface Parametrics

Class A (High Performance)				Class B (Wide Margin)			
Vih(DC)_min	=	Vref	+ 0.07 * VDD	Vih(DC)_min	=	Vref	+ 0.14 * VDD
Vih(DC)_max	=	VDDQ	+ 0.10 * VDD	Vih(DC)_max	=	VDDQ	+ 0.10 * VDD
Vil(DC)_max	=	Vref	- 0.07 * VDD	Vil(DC)_max	=	Vref	- 0.14 * VDD
Vil(DC)_min	=		VSS	Vil(DC)_min	=		VSS
Vih(AC)_min	=	Vref	+ 0.14 * VDD	Vih(AC)_min	=	Vref	+ 0.25 * VDD
Vih(AC)_max	=	VDDQ	+ 0.15 * VDD	Vih(AC)_max	=	VDDQ	+ 0.15 * VDD
Vil(AC)_max	=	Vref	- 0.14 * VDD	Vil(AC)_max	=	Vref	- 0.25 * VDD
Vil(AC)_min	=	VSS	- 0.15 * VDD	Vil(AC)_min	=	VSS	- 0.15 * VDD

Although it is commonplace to standardize output driver currents and output driver voltages (V_{oh} , V_{ol}), this standard will refer to output driver impedances. Through reference to driver impedance the driver characteristics will become easier to define and the resultant driver behavior under various loading conditions will be easier to predict. For the expected values for driver impedance and the parametrics associated with the drivers (see section 4).

2.2 Interoperability

It is expected that a group of devices of different supply voltages VDD will communicate with a common communication voltage VDDQ which is equal to or less than VDD_{low}, the lowest supply voltage of the group. Although it is desirable that chips of supply voltage VDD operate over the largest possible range of VDDQ, to meet this standard it is sufficient that chips of VDD specified in table 2-3 support communication at the associated values of VDDQ, with the Vil, Vih specifications of table 2-2.

Table 2-3 — Relationship between VDD, VDDQ, and Vref

VDD	VDDQ	Vref
1.5 V	1.5 V, 1.2 V, 1.0 V	0.75 V, 0.6 V, 0.5 V
1.2 V	1.2 V, 1.0 V, 0.8 V	0.6 V, 0.5 V, 0.4 V
1.0 V	1.0 V, 0.8 V	0.5 V, 0.4 V

The relationship is roughly $VDD \geq VDDQ \geq 0.6 \times VDD$

2.2 Interoperability (cont'd)

Similarly the I/O drivers associated with a semiconductor device operating with external voltage VDD must be capable of providing an output voltage, satisfying the input requirements V_{il} and V_{ih} of table 2-2 for a receiver configured for any associated VDDQ in table 2-3, at the specified impedance. Separate VDDQ pins are recommended but not required. Separate VSS and VSSQ pins are acceptable but not required.

3 Flexible I/O interface receiver

3.1 Receiver types

A receiver covered in this section differentiates between a voltage sampled at the receiver input being greater or less than some switch point or reference voltage V_{ref} . To provide some immunity to noise and various factors that effect receiver operation such as temperature, voltage, and circuit feature sizes and material properties, the switch point is in general associated with a range, described by its limits V_{ih_min} at the high end and V_{il_max} at the low end. Section 1 and 2 of this document defines these numbers for various supply voltages VDD and I/O voltages VDDQ where VDDQ is less than or equal to VDD. The center of this range, $(V_{ih_min} + V_{il_max})/2$, is the switch point or reference voltage. For fixed supply voltage VDD, the switch point or reference voltage changes with VDDQ.

One class of receivers relies on this reference voltage being supplied externally, on one of the pins of the package housing the chip. When a reference voltage is defined this way we use capital letters **VREF** to denote this. A second class of receivers generates the reference voltage internally. We use the smaller case **Vref** to denote this.

This section covers receivers which can operate with either an external **VREF**, or internal **Vref**, voltage reference. These or any other circuit technique may be used for creating receiver circuits covered in this section.

3.2 Interoperability

To be compatible with this standard, any chip with an external voltage reference **VREF** must be capable of also operating with an internal voltage reference **Vref**. The switch from external to internal voltage reference is made by making the **VREF** voltage = VDD. This is otherwise known as **Must Connect To VDD (MCVDD)**. To be compatible with this standard, the signal pin **VREF** of the semiconductor chip would be labeled **VREF / MCVDD**. The value of **VREF** or **Vref** and the associated value of V_{il} and V_{ih} as specified in sections 1 and 2 of this document.

3.2 Interoperability (cont'd)

The internal **Vref** must be capable of changing with VDDQ, the communication voltage, as specified in sections 1 and 2 of this document. Similarly the external voltage **VREF** must be variable over the range of supported VDDQ.

The value of the **Vref** may be changed through a register accessed either through mode bits, a JTAG interface, or any other user programmable interface. In this case the default **Vref** for a semiconductor chip operating with supply voltage VDD is the lowest value of the reference voltage specified in sections 1 and 2 of this document.

The value of the internal **Vref** may be changed in direct response to a change in VDDQ through an internal voltage sampling circuit (self programmed). In this case there is no default value for **Vref**.

4 Flexible I/O interface driver impedance

4.1 Impedance specification

The impedance, or ratio of the output voltage to the output current, of a high speed I/O driver circuit is in general a variable which changes, often in a non-linear fashion, with the supply voltage, chip temperature, and circuit feature sizes and material properties. Nevertheless, it is possible to define an "ON" impedance and range, intended to cover the range of operating voltages and chip process variations, which is measured while the chip is delivering a voltage pulse to a matched impedance load. Thus a driver circuit of nominal impedance Z_{drv} would create a voltage $V_{load} = VDDQ/2$ across a load resistor $R = Z_{drv}$, where VDDQ is the communication voltage for a chip operating at supply voltage VDD. The supply Voltage VDD and communication voltage VDDQ are related as described in sections 1 and 2 of this document. Alternatively, the load resistor can be replaced by a transmission line of nominal impedance $Z_{line} = Z_{drv}$, and the driver will create a voltage VDDQ at the end of the unterminated line.

4.2 Impedance selection

The driver impedance can be selected to drive either a single load (matched to minimum transmission line impedance) or multiple loads. There are two methods for specifying driver impedance. One or the other method should be selected for compliance with this standard.

4.2 Impedance selection (cont'd)

Method I

Impedance is specified through the use of a resistor (RZ) connected between pin ZQ and ground. Here $RZ = 5x$ the desired impedance. Since these drivers may be used in a variety of specialized device networks, we define 3 operating ranges for this type of driver. To comply with this document, at least one operating range must be supported. Multiple, or larger, operating ranges are acceptable. The three ranges for a driver impedance programmed with an external resistor are:

Type	Range	Tolerance
<i>Low Impedance</i>	10 - 30 Ohms	+/- 20%
<i>Mid Range Impedance</i>	25 - 60 Ohms	+/- 15%
<i>Line Impedance</i>	40 - 60 Ohms	+/- 10%

The impedances must be maintained to at least the specified accuracy over the full range of allowed operating conditions of VDD, VDDQ, and Temperature.

Method II

Alternatively, impedance may be specified through an internal register accessed either through mode bits, a JTAG interface, or any other user programmable interface. At least one of the below impedance modes must be supported. The impedances specified are for nominal operating conditions and cannot vary by more than +45% /-35% (factor of 2.2 from worse case to best case) over the full range of operating conditions. The 4 modes are:

Type	Nominal Z_drv	Tolerance (%)	Tolerance (Ohms)
Weak	45 Ohms	+45% 1-35%	29 to 65 Ohms
Normal	22 Ohms	+45%/-35%	14 to 32 Ohms
Strong	10 Ohms	+45% 1-35%	7 to 15 Ohms
Very Strong	5 Ohms	+45% 1-35%	2 to 7 Ohms

Support of multiple of these impedance modes is encouraged but not required. Other impedance ranges and tolerances may be optionally supported. Nominal impedances for both pull-up and pull-down impedances should be equal. The pull-up impedance is measured by placing a load resistor (R_load) of value equal to the nominal driver impedance (Z_drv) between the output pin and VDDQ. The pull-down impedance is measured by placing a load resistor of value equal to the nominal driver impedance between the output pin and ground.

In either case the impedance is measured using the voltage divider equation:

$$\text{Voltage_across_resistor} / \text{VDDQ} = R_load / (Z_drv + R_load).$$

Thus the steady-state driver impedance is measured when driving a matched load.

